REMARKS

This Amendment is in response to the Office Action dated June 4, 2007, in which claims 1-7 and 16-20 initially rejected, and claims 8-15 were withdrawn as being directed to a non-elected invention. Applicants respectfully request reconsideration and allowance of all pending claims in view of the above-amendments and the following remarks.

I. SPECIFICATION

In Section 1 of the Office Action, the Examiner requested that Applicant update the cross-reference to include the serial number and filing date of the cross-referenced application. However, Applicant previously filed a Preliminary Amendment on July 19, 2004, which included the requested information. In any event, Applicant has re-submitted the requested amended paragraph as shown above.

II. CLAIM REJECTIONS UNDER §101

Claims 1-7 and 16-20 were rejected under §101 as allegedly being directed to non-statutory subject matter. Claims 1 and 16 are amended to state that the software block is stored in computer-readable memory, which, per se, makes the claims statutory.

Per the Interim Guidelines, functional descriptive material is statutory when recorded on some computer-readable medium, since it becomes structurally and functionally interrelated to the medium and permits the function of the descriptive material to be realized.

III. CLAIM REJECTIONS UNDER §112

Claims 2, 17 and 20 were rejected under §112, second paragraph, as being indefinite.

Claims 2 and 17 are amended as suggested by the Examiner.

Claim 20 already defines the interrupt configuration and is amended to state that the interrupt configuration is adapted to replace the variables with "values that define unique interrupt connections for each instantiation".

Thus, claims 2, 17 and 20 are believed to be sufficiently definite.

none of the claim amendments have been made in view of or to distinguish over any prior art reference.

IV. CLAIM REJECTIONS UNDER §102

Claims 1-7 and 16-20 were rejected as being allegedly anticipated by Bowen U.S. Publication No. 2002/0100029.

Bowen generally relates to a process of taking C code and splitting the code between hardware and software. For the hardware, RTL is generated, synthesized and put into an FPGA. The software is put into machine code. The hardware compiler produces "a register transfer level description for configuring configurable logic resources".

In section 7, the Office Action refers the background section of the present application. The background (problem) of Bowen is different than what the present application is addressing. Bowman addresses the designer's issues of how much of the design should be software and how much should be in hardware.

The present patent application addresses how IP components (in this case software components) can be easily reused in different chips and to configure multiple instantiations of a peripheral device in a system. The abstraction layers in claims 1-7 and 16-20 are all software.

As described in the specification on page 45,

The device hardware abstraction layer (HAL) header and C code files provide a general data structure of a whole register set of the peripheral. This general data structure can then be adapted readily for reuse, simply by utilizing device-specific function calls.

The platform HAL header and C code files define base addresses for each instantiation of a peripheral device. In this way, utilizing code blocks, registers can be defined by the platform HAL by calling initialization functions with a memory location, which is then used by the initialization function to initialize the registers at the memory location provided. Thus, the platform HAL can utilize the same software block to perform the same initialization routine for multiple instances, simply by providing a different location to the initialization block each time.

A. **Claims 1 and 16**

Claims 1 and 16 include a "device hardware abstraction layer" and a "platform hardware abstraction layer".

1. "device hardware abstraction layer"

With respect to the "device hardware abstraction layer", the Office Action refers to Bowen's figure 2, element 212 of "behavioral synthesis" and to paragraph [0053]. In paragraph [0053], Bowen states,

> "In operation 102, the system receives a behavioral description of the electronic system and, in operation 104, determines the optimal required functionality between hardware and software. In operation 106, that functionality is partitioned preferably while varying the parameters (e.g. size or power) of the hardware and/or software."

In contrast to Bowen, the claimed "device hardware abstraction layer" is in software and is not getting mapped to hardware. Bowen does not disclose a device hardware abstraction layer that defines offset values for registers of a peripheral device or a data structure for the peripheral device.

The claim mentions 'peripheral devices', to refer to a device that the software needs to control/configure (e.g., something that has registers), for example. The examiner just lists the elements of figure 10 to say Bowman teaches about peripheral devices.

However, the Office Action shows no support for the claimed "device hardware abstraction layer" recited in claims 1 and 16.

2. "platform hardware abstraction layer"

With respect to the platform abstraction layer, the examiner is again referencing parts where the software is mapped to hardware and synthesized to gates (e.g., Fig. 2, element 214, RTL Synthesis).

What we are referring to is how a "higher" layer of abstraction (the platform abstraction layer) can use a lower layer of abstraction (the device abstraction layer) to "talk to" (i.e. control/configure) something in hardware.

Bowen to not disclose a "platform hardware abstraction layer".

Bowen to not disclose "a platform hardware abstraction layer" that defines "an address map" of a system comprising multiple instantiations of a peripheral device.

Bowen to not disclose a "platform hardware abstraction layer" that is "adapted to initialize each instantiation of the peripheral device via calls to the device hardware abstraction

layer" within the context of claim 1.

These elements have been ignored in the Office Action.

Independent claims 1 and 16 are clearly not anticipated by Bowen.

B. **Claims 2 and 17**

For claims 2 and 17, the phrase 'during initialization' refers to initialization of the "system", which contains multiple instantiations of a peripheral device.

In claim 2, for example, the device hardware abstraction layer comprises "memory register locations adapted to be configurable during initialization of the system". According to claim 1, the platform hardware abstraction layer adapted to initialize each instantiation of the peripheral device via calls to the device hardware abstraction layer.

Bowen does not disclose abstraction layers, where the device abstraction layer has configurable memory register locations that are configured by the platform abstraction layer.

Further, Bowen dies not disclose a device hardware abstraction layer having an interrupt configuration, which is configured for the peripheral device during initialization of the system.

In contrast, Paragraph [0170] of Bowen refers to tuning things that will be in hardware. This is part of Bowen's example 1. Applicants do not understand why the Office Action mentions the OOP components of Bowen.

Claims 2 and 17 are therefore not anticipated by Bowen.

Similarly, the remaining claims recite further elements and limitations that are not anticipated by Bowen. Applicants therefor respectfully request that the rejection of claims 1-7 and 16-20 under §102(b) be withdrawn.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 12-2252.

Respectfully submitted,

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